(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **10335659 A**

(43) Date of publication of application: **18.12.98**

(51) Int. Cl **H01L 29/78**

(21) Application number: **09147794**

(22) Date of filing: **05.06.97**

(71) Applicant: **TOSHIBA MICROELECTRON CORP TOSHIBA CORP**

(72) Inventor: **TOYOMARU YOUKO**
KAGEYAMA MOKUJI
TSUCHIYA NORIHIKO

(54) SEMICONDUCTOR DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To obtain a MOSFET which is enhanced in operation speed as high as possible even if it is formed on a wafer with a surface of step-terrace structure.

SOLUTION: A semiconductor device is equipped with a MOSFET formed on the step of a silicon substrate, the direction in which a step provided to the surface of the silicon substrate extending under the gate electrode of the MOSFET makes an angle θ with the other direction in which carriers flow from the source region to drain region of the MOSFET, and provided that the gate length of the gate electrode is represented by L, the length of a terrace provided to the surface of the silicon substate is represented by d, θ, L, and d are so set as to a satisfy a formula, L/d2|k/sin θ|, (-90°2θ290°, k25).